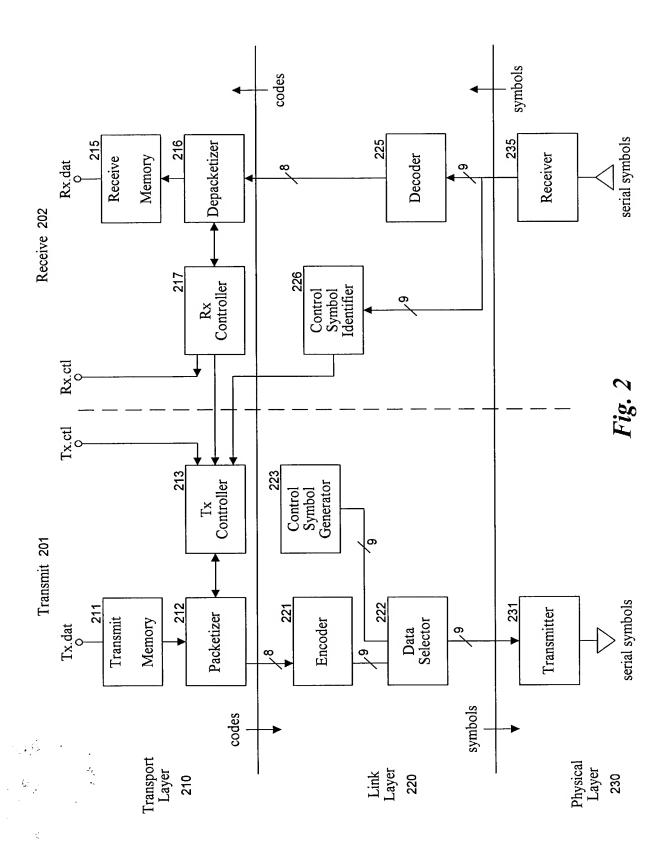
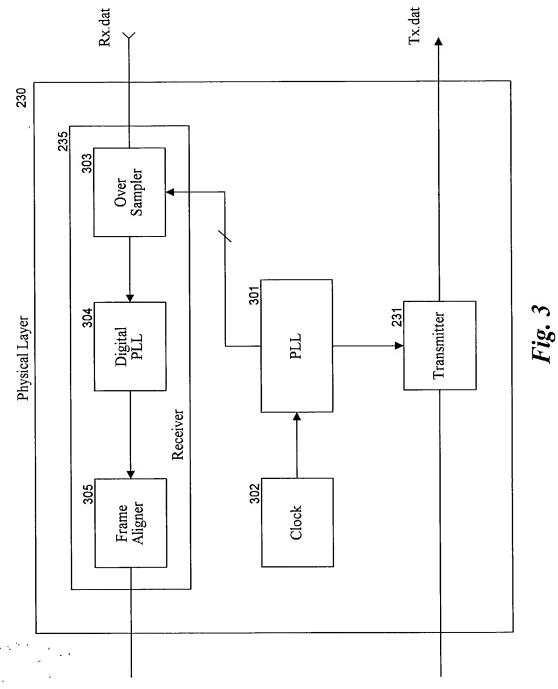
120 Data Store Device	125 Transport Layer	Link Layer Physical	Layer	• • •	120 Data Store Device	125	Fransport Layer	Link Layer	Physical Layer
			140						140
130	135 Transport Layer	Link Layer Physical	Layer	hing /ork		135	Transport Layer	Link Layer	Physical Layer
	135 Transport Layer	Link Layer Physical	Layer	Switching Network		135	Transport Layer	Link Layer	Physical Layer
			140						140
110	115 Transport Layer	Link Layer Physical	Layer	• • •	110	115	Transport Layer	Link Layer	Physical Layer
Host					Host				

Fig. 1





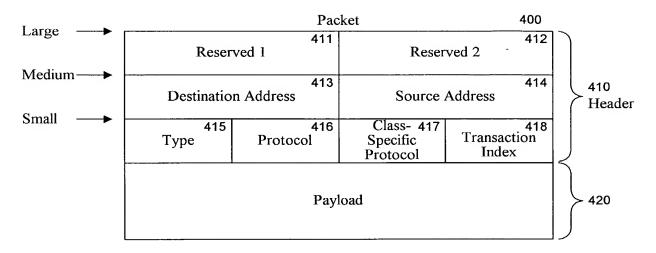
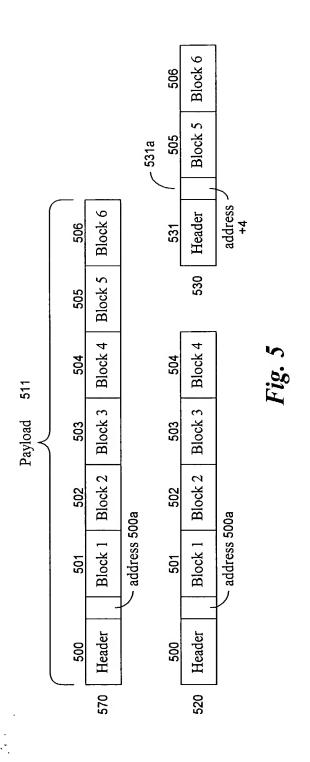
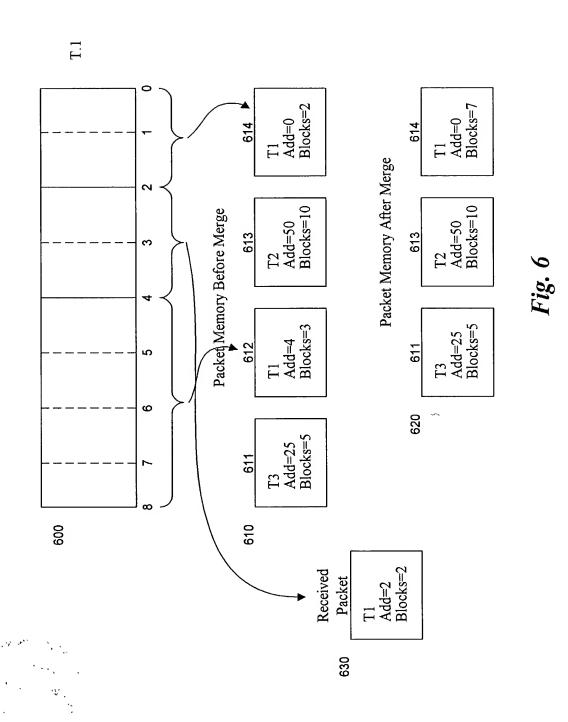


Fig. 4





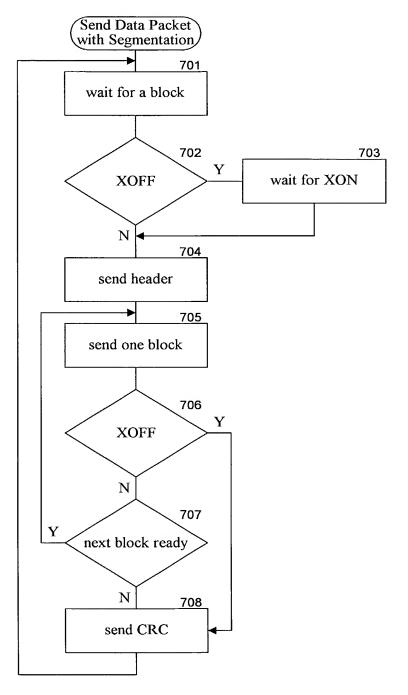


Fig. 7

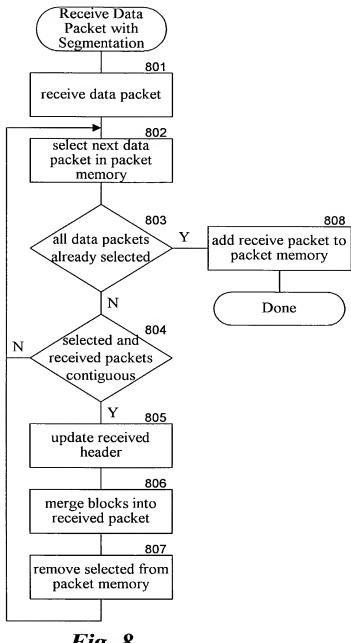
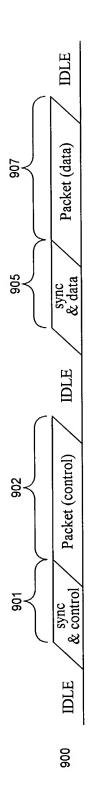


Fig. 8



sync & packet type

Fig. 9A

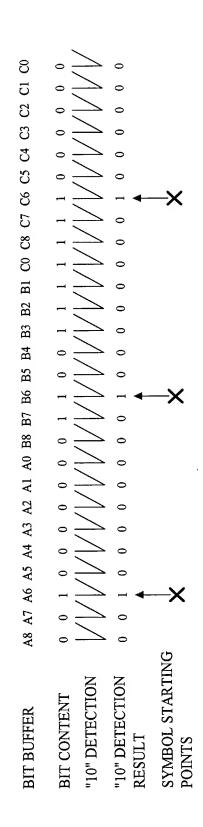


Fig. 9B

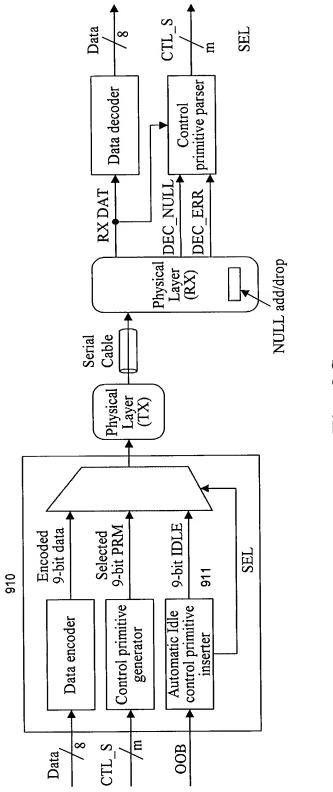
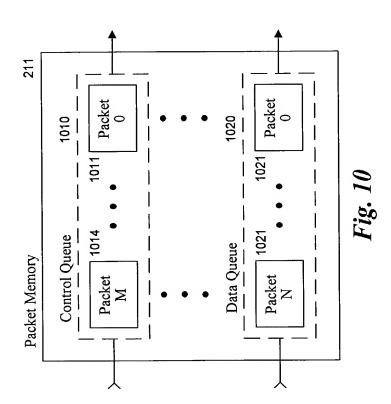


Fig. 9C



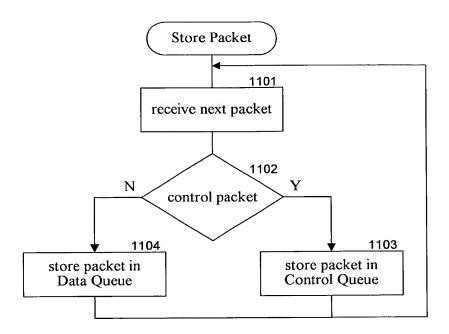


Fig. 11

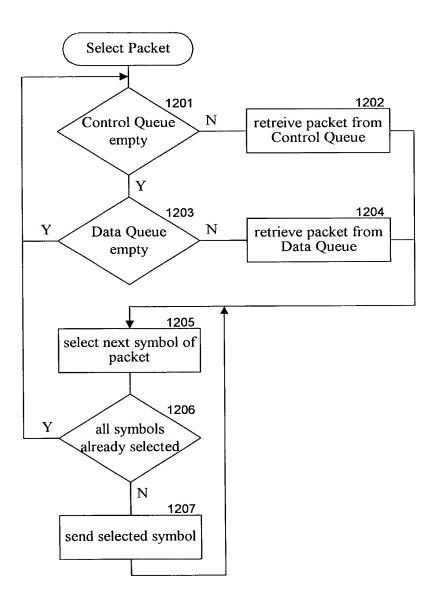


Fig. 12

	, L	IDLE
1305	data	packet (cont'd)
1304	· _	continue
1303	control	packet
1302		Preempt
1301	data	packet /
		DLE
	1300	

Fig. 13

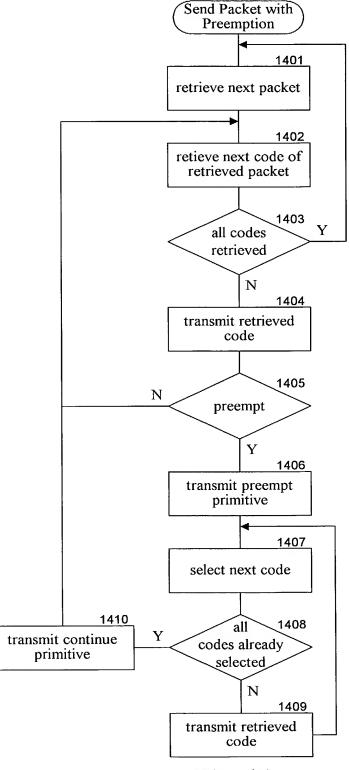


Fig. 14

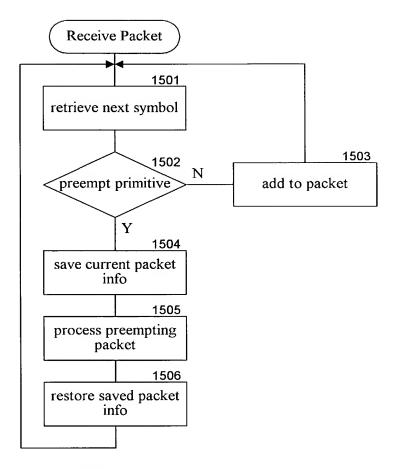


Fig. 15

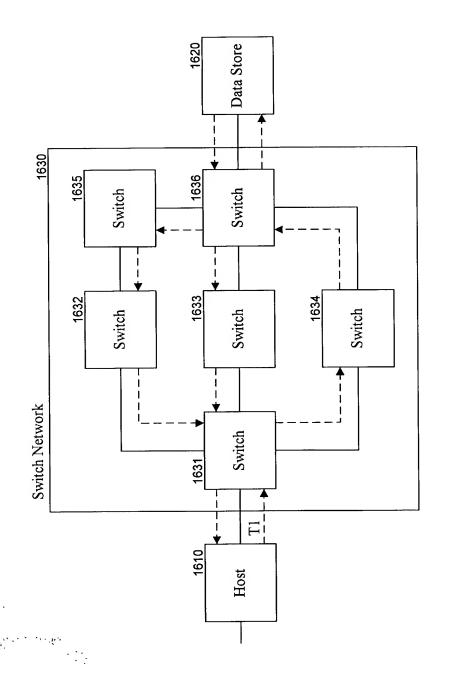


Fig. 16

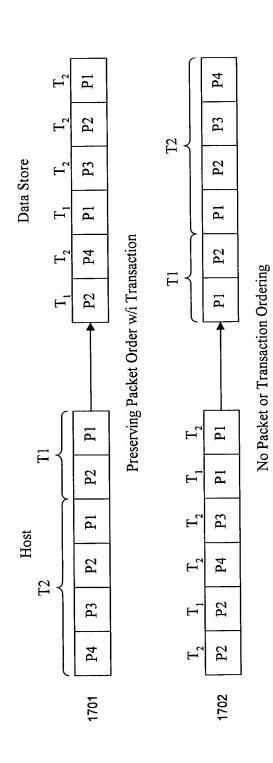


Fig. 17

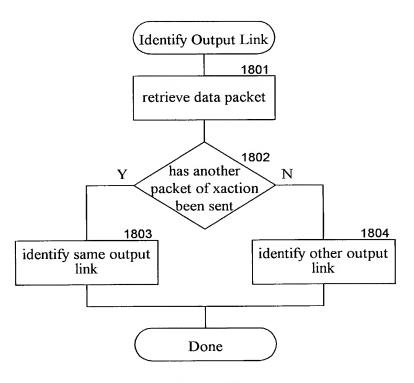
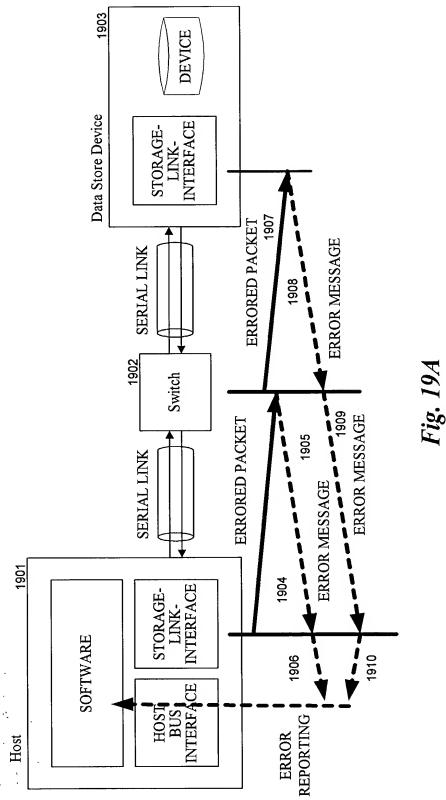
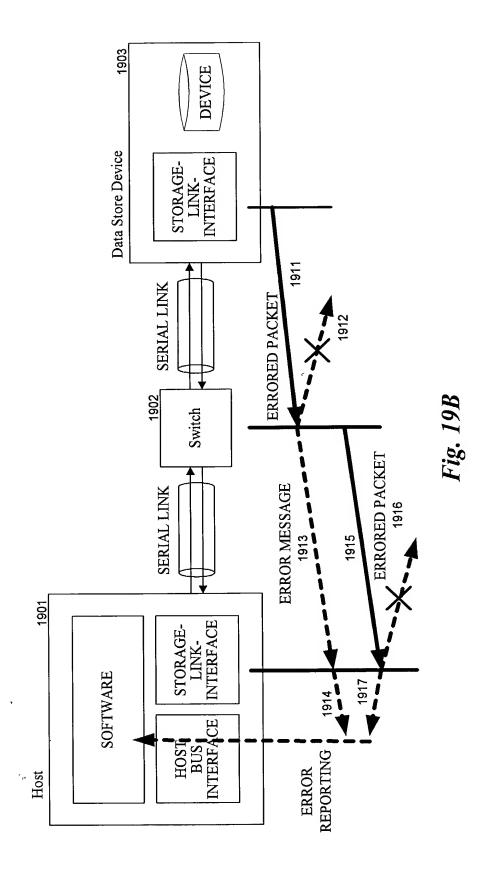


Fig. 18





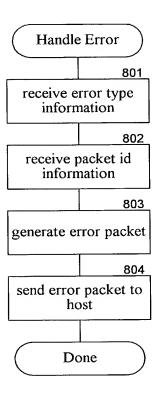


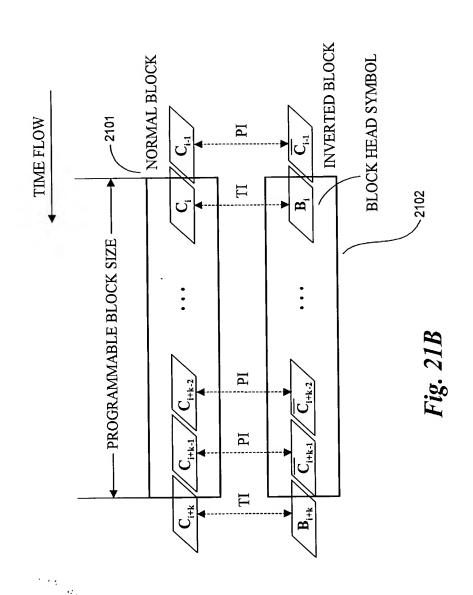
Fig. 19C

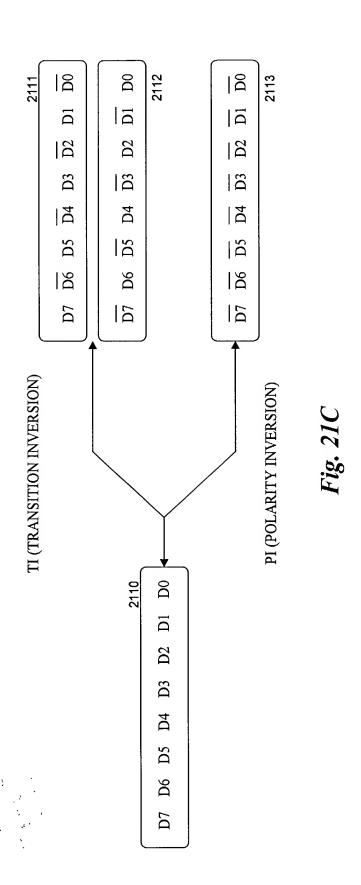
8b code	9 bit symbol			
0000 0000	101010101			
0000 0001	101010100			
0000 0010	101010111			
0101 0101	001010101			
0111 0110	001110110			
0111 0111	100100010			
:	110101010			

Fig. 20

Symbol 4	110101010		001010101
Symbol 3	101010111	Bit Inversion	010101000
Symbol 2	001110110		10001001
Symbol 1	101010101	Alternate Bit Inversion	000000000
	Block Disparity	+	

Fig. 21A





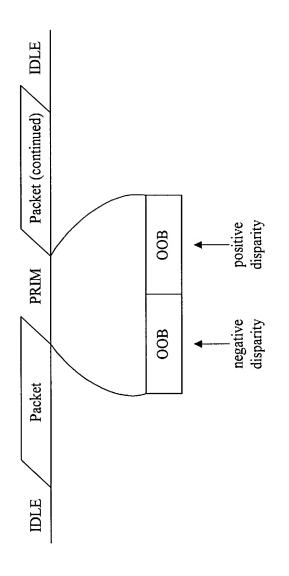


Fig. 22

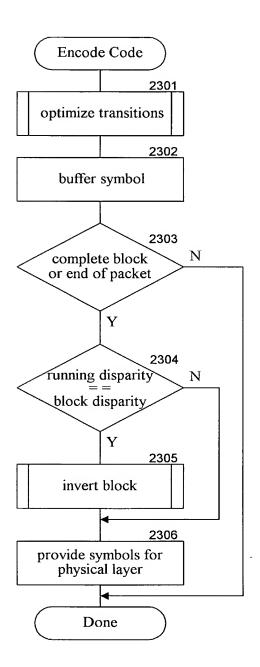


Fig. 23

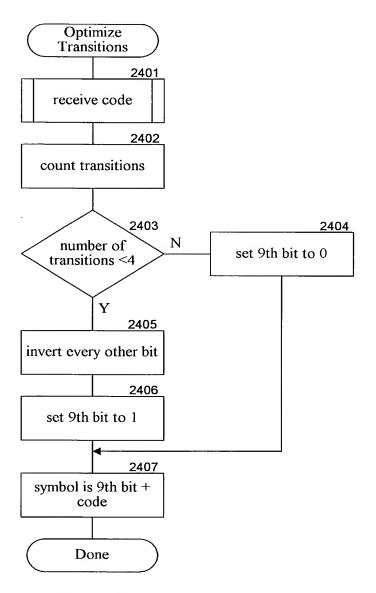


Fig. 24



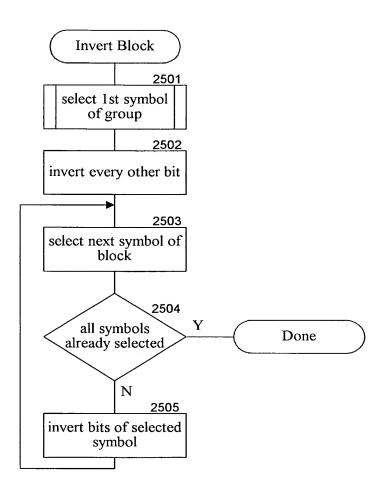
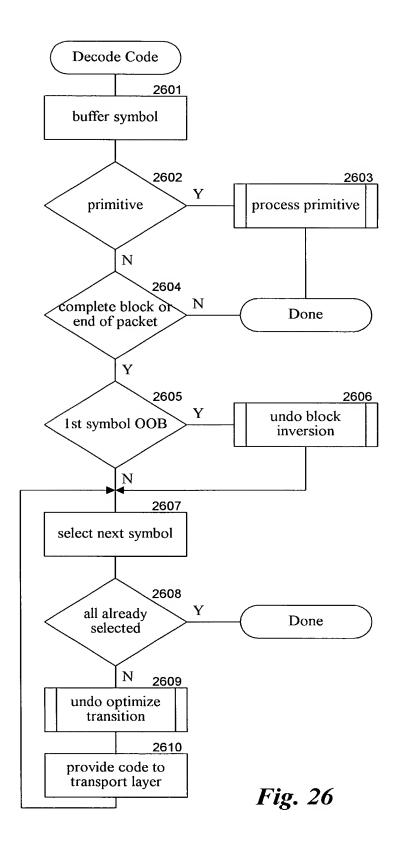


Fig. 25



A second

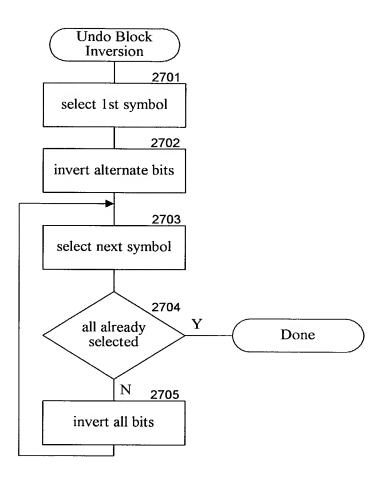


Fig. 27

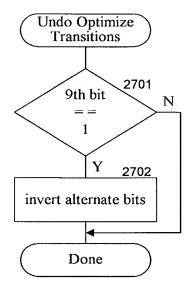


Fig. 28

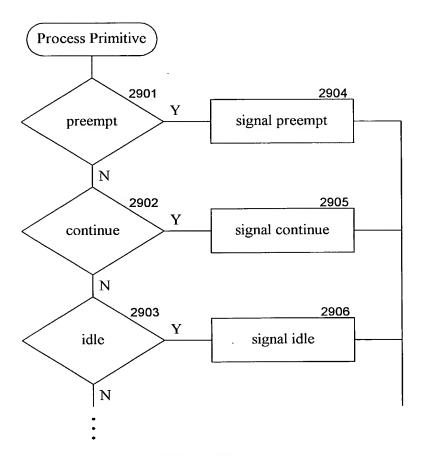
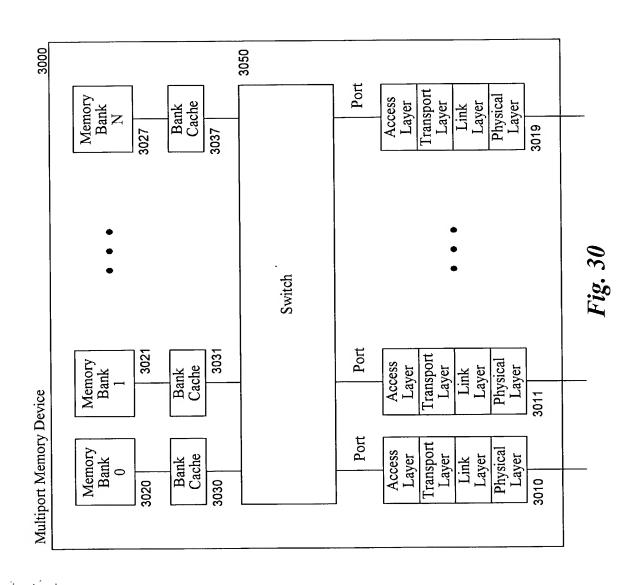
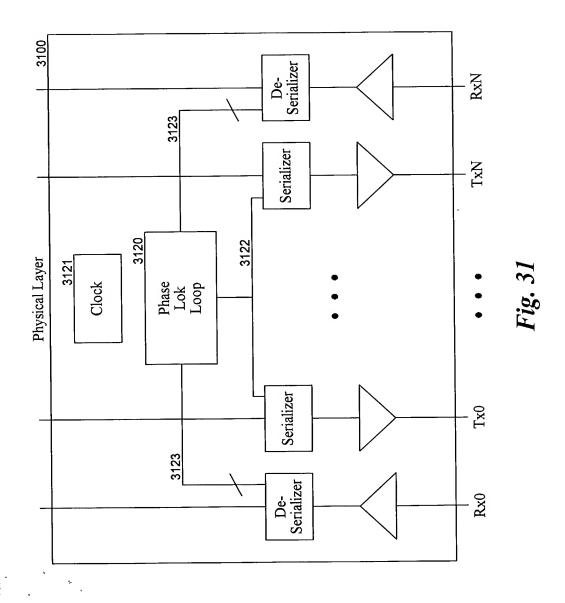


Fig. 29





Output Queue 3202	Data	110			1011	
	Valid Port Data	3			3	• • •
	Valid	1	0	0	1	
	'					
3201	Data		101	1000 1110		
Input Queue	R/W Address	1000	4000	1000	2000	
	R/W	R	M	W	R	• • •
	Port	3	4	3	3	

Fig. 32

Section 1.

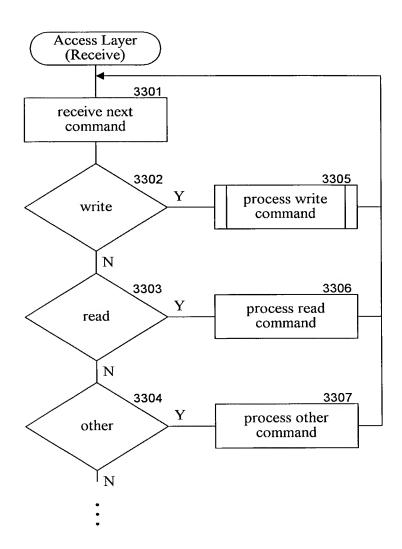


Fig. 33

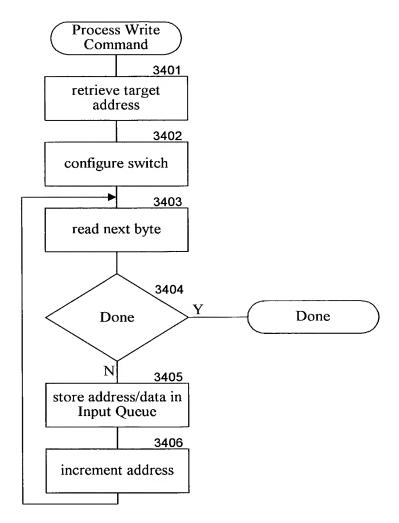


Fig. 34

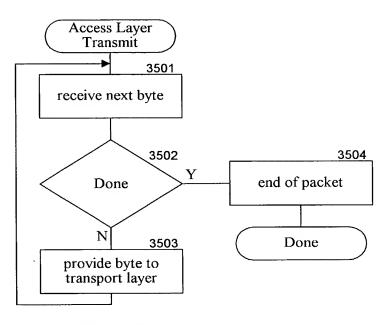
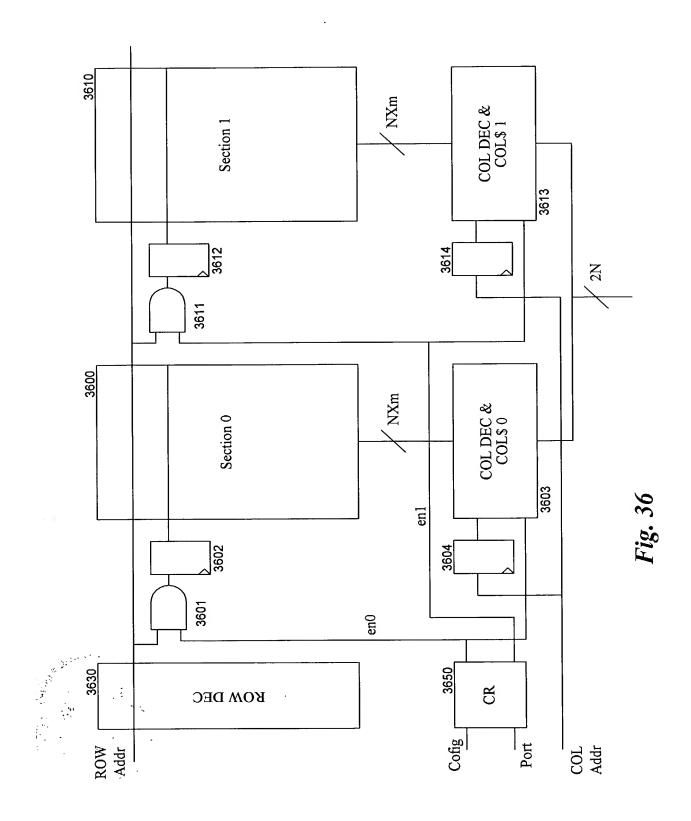


Fig. 35



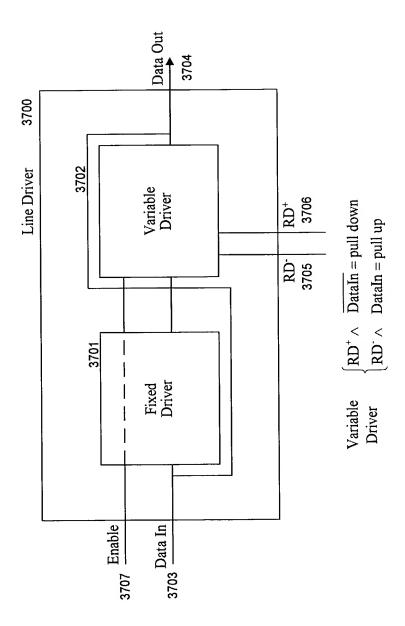
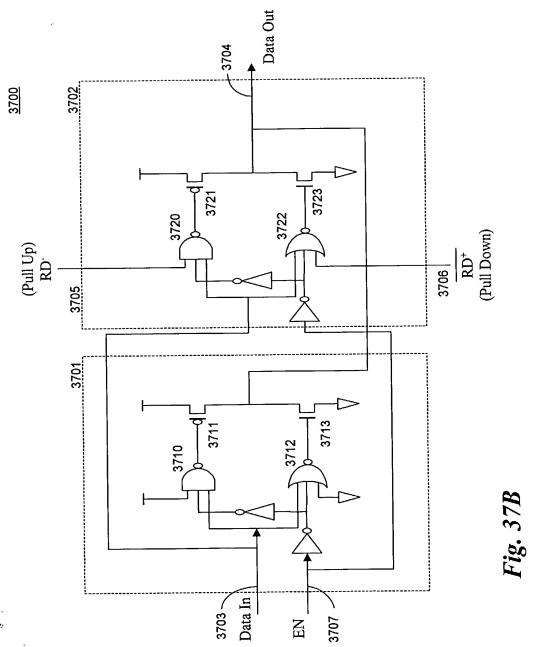
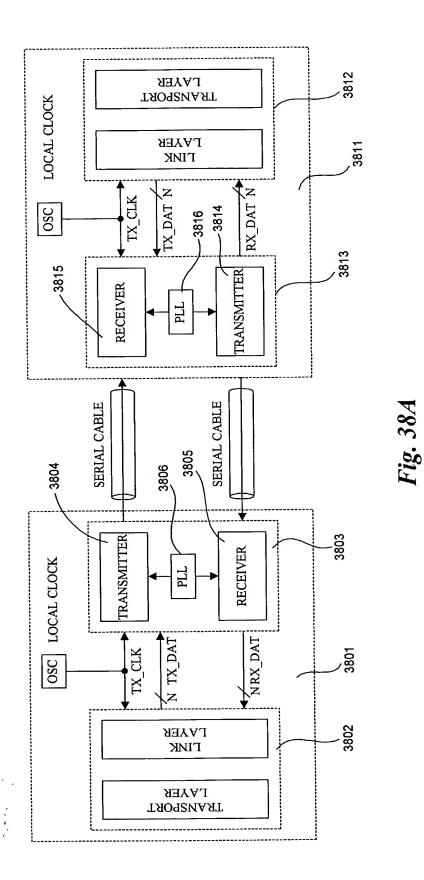


Fig. 37A



1867 (1881) 1867 (1881)

.



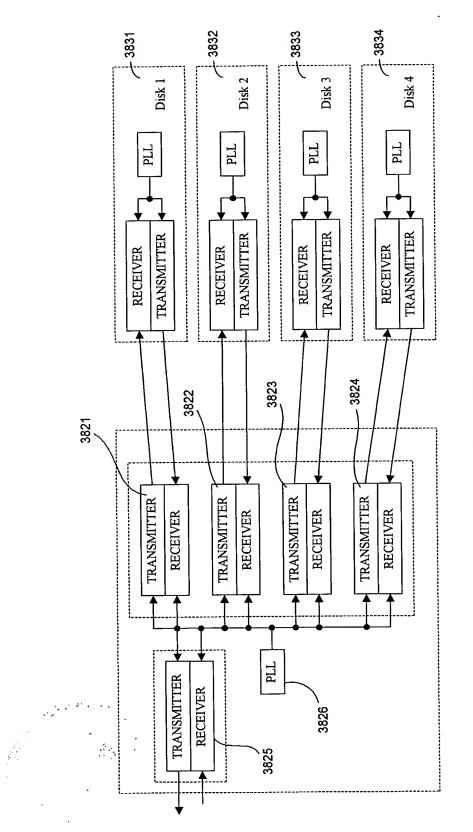
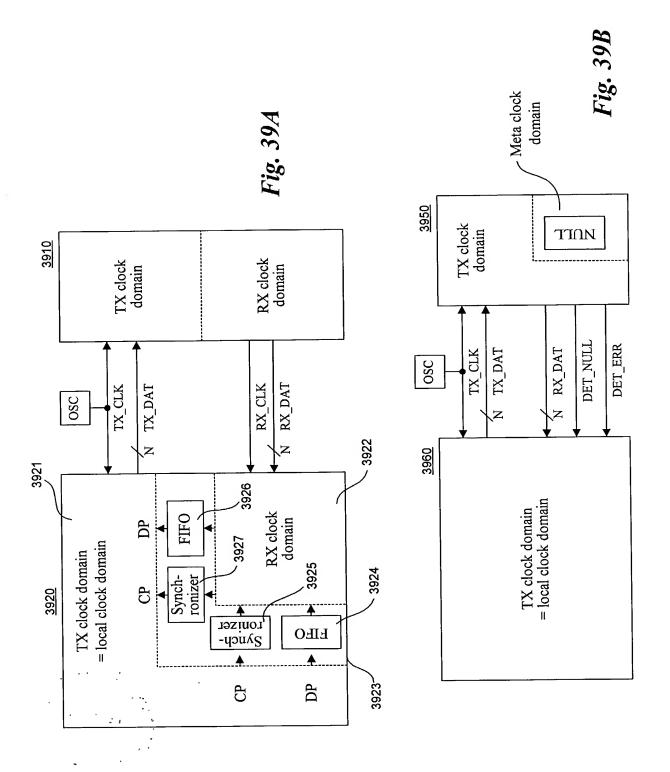
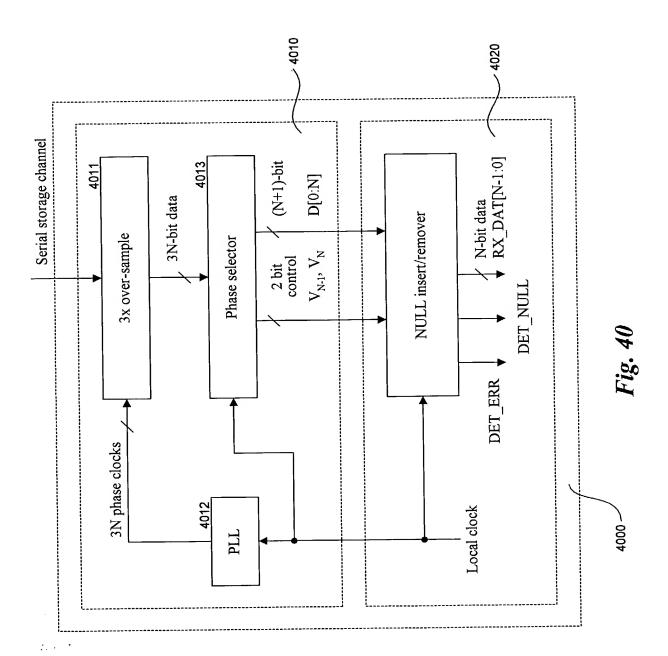


Fig. 38B





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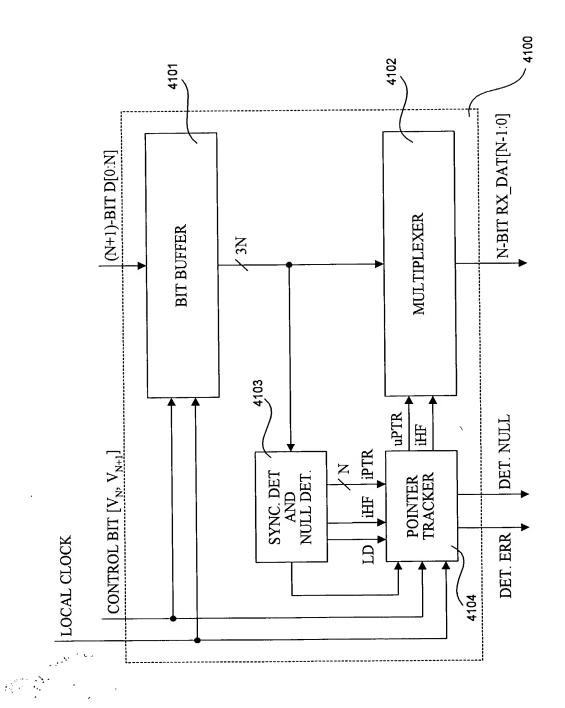
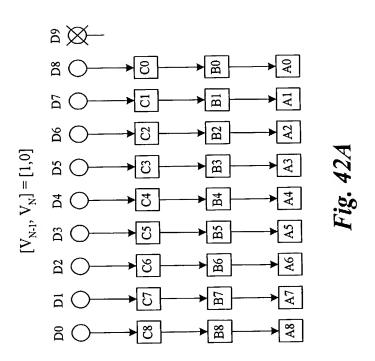
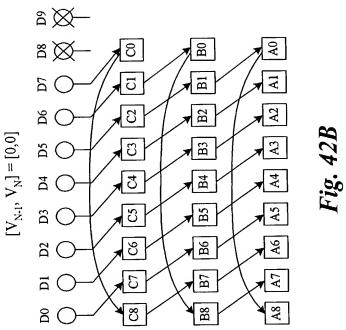
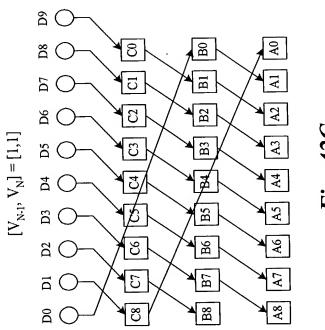


Fig. 41







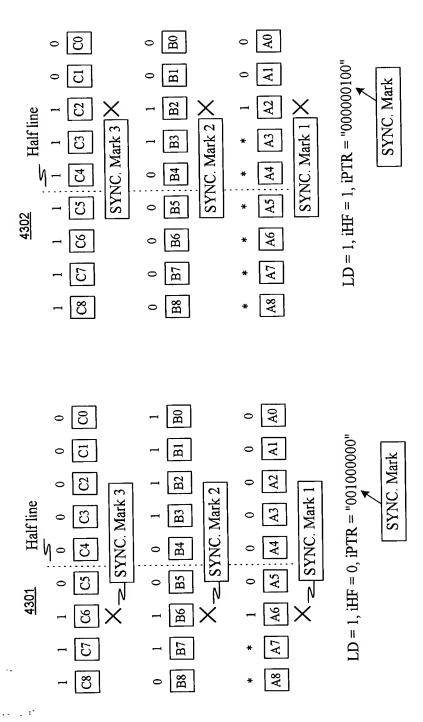


Fig. 43

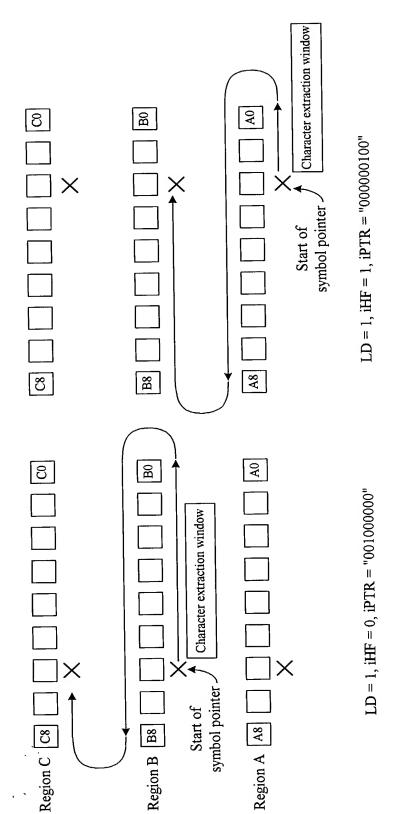
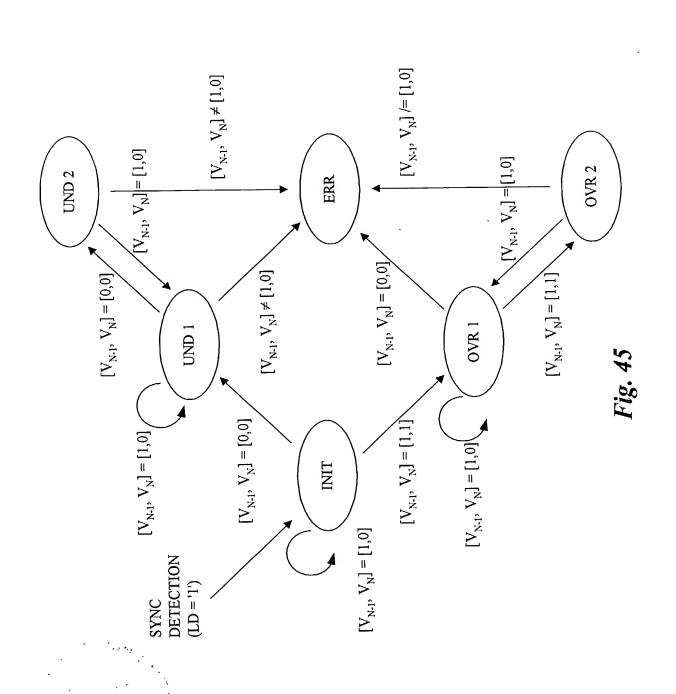


Fig. 44



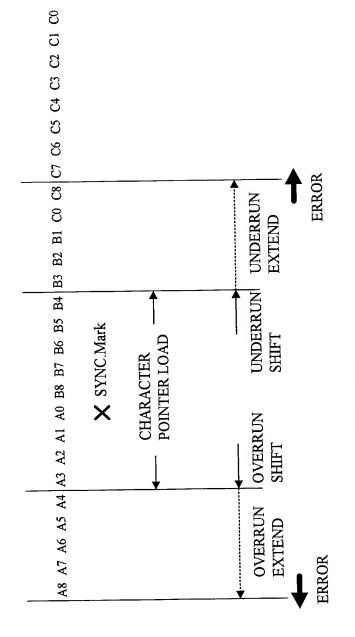
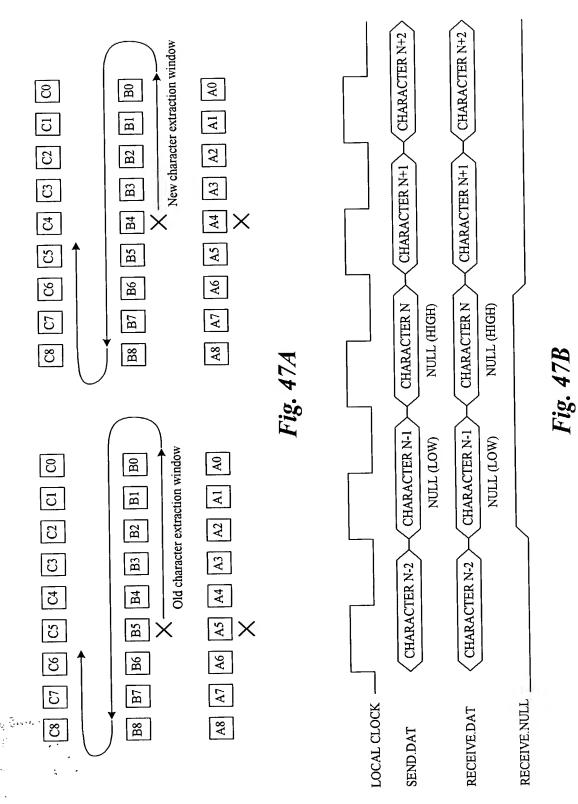
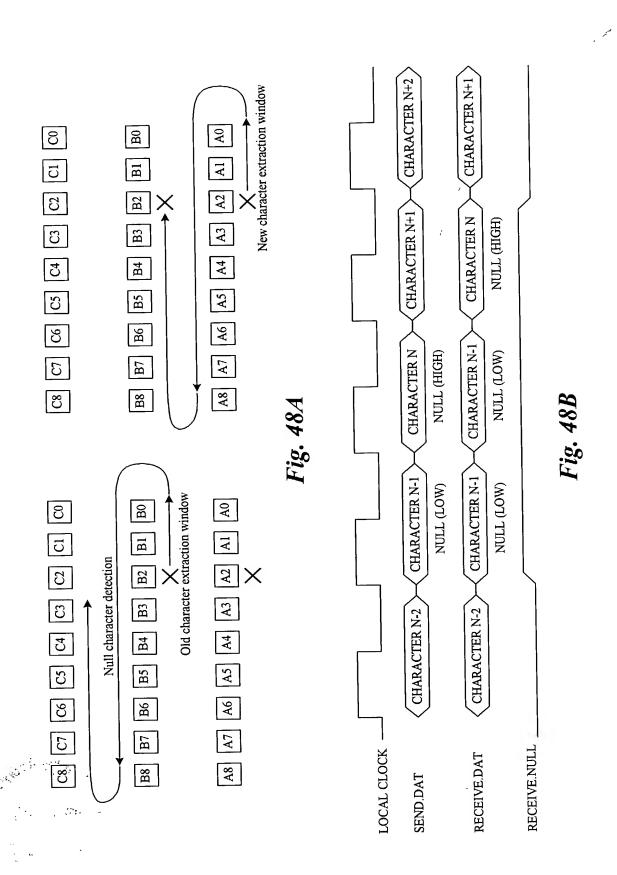


Fig. 46





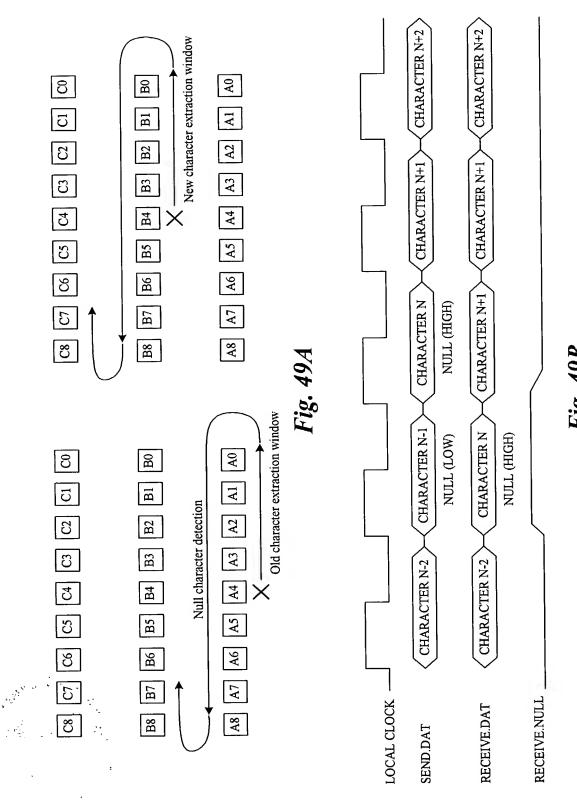


Fig. 49B